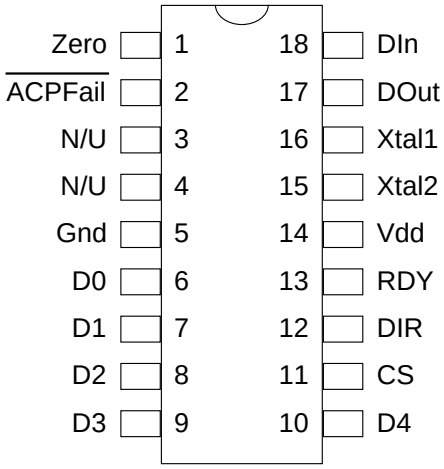
Micromint Chips

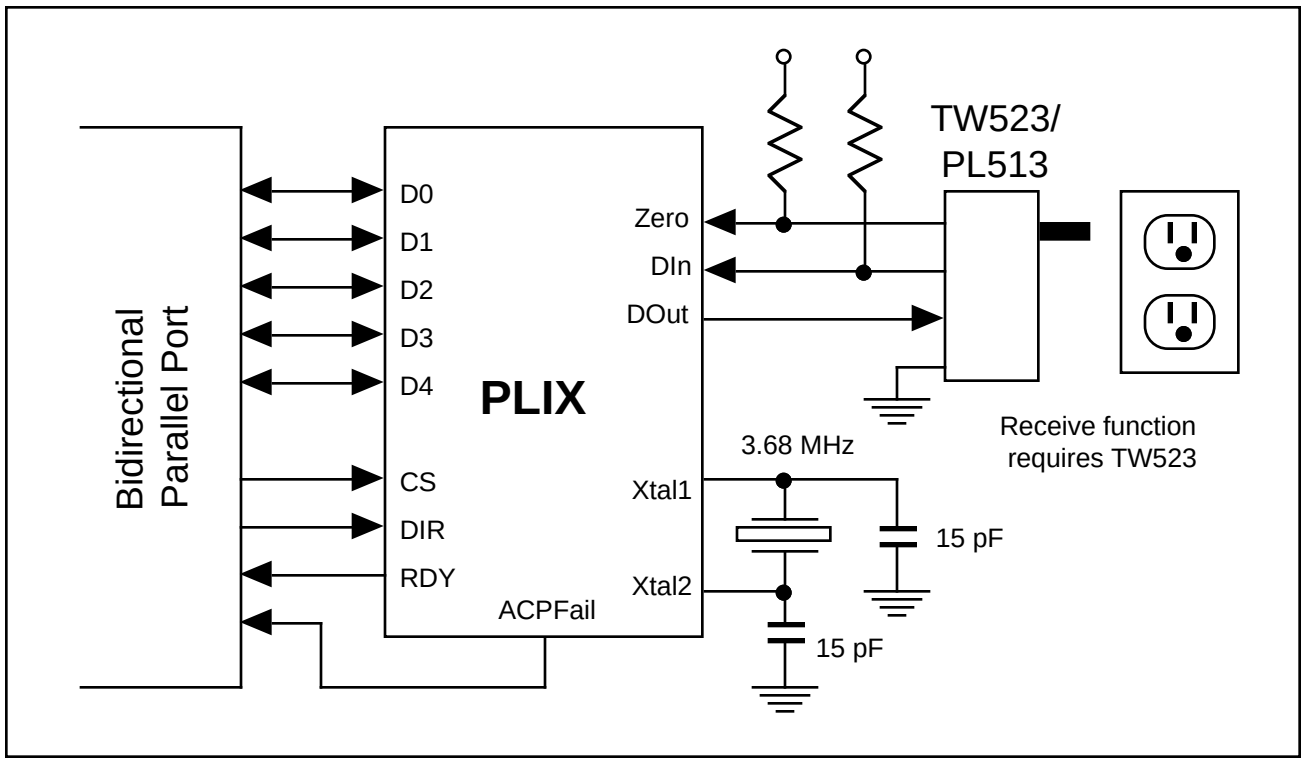
# PLIX™

## Power Line Interface for X-10™

### Features

- Complete interface between a microprocessor and an X-10 TW523 or PL513 module
- Performs all transmit and receive functions
- Detects loss of AC power in a battery-powered system and reports it to the microprocessor
- Interfaces to a single 8-bit bidirectional parallel port
- Low parts count (requires just two resistors, two capacitors, and a crystal)
- Low power consumption (1.8 mA typical @ 5 V)
- Voltage operating range: 4.0 V to 5.5 V
- Standard 18-pin, 0.300″ DIP package




 X-10 is a trademark of X-10 (USA), Inc. 

## The X-10 Power Line Control System

The X-10 system was first introduced in the late 1970s as a simple, power-line-based, remote control system. Commands are transmitted over the AC power lines already installed in virtually all houses in the United States and other countries, eliminating the need to pull extra wires.

To use the X-10 system, the user sets a house code (A–P) and a unit number (1–16) on a control module and plugs the module into a wall outlet. The user then plugs a lamp or appliance into the module. To control the module, a remote control console is set to the same house code, then buttons are pressed to select the particular module and to issue it commands.

The X-10 system has been greatly expanded since it was first introduced. In addition to modules, there are also wall switches, switched outlets, chimes, relays, motion detectors, and other devices available that are X-10 compatible.

A natural extension to such a control system is to allow a computer to send and receive X-10 commands to and from the power line. Computers generally aren't designed to be connected to the power line (beyond their simple power supply), so great care must be taken when doing so. The PL513 and TW523 computer interface modules provide a safe, UL-approved, optoisolated connection to the power line and allow a computer to send and, in the case of the TW523, to receive X-10 commands.

The main drawback of the PL513 and TW523 has been the code complexity needed to drive the modules. The modules provide a very basic interface, leaving all the complex timing, encoding, and decoding to the host microprocessor. In order to handle the tricky timing involved, assembly language routines are a virtual necessity.

PLIX has been designed to remove the burden of complex programming from the designer. PLIX uses a simple parallel port interface that can be accessed from virtually any programming language including interpreted BASIC. It takes care of all the complex timing involved in sending and receiving commands to and from the power line. It also tells you when AC power has been lost in a battery-backed system.

## Pin Descriptions

Zero—Zero-crossing detect input from the PL513/TW523. Connect to pin 1 on the module and pull up to Vdd through a 10k resistor.

DIn—Data input from the TW523. Connect to pin 3 on the module and pull up to Vdd through a 10k resistor. When using a PL513, this pin should be tied to Vdd.

DOut—Data output to the PL513/TW523. Connect to pin 4 on the module.

ACPFail—AC power fail detect output to the computer. When no zero crossing has been detected by the PL513/TW523 for 20 milliseconds, this pin goes low to indicate AC power has failed or the PL513/TW523 has been unplugged. When power is restored, ACPFail immediately goes high.

D0–D4—Data path between PLIX and the computer's bidirectional parallel port. Data direction is determined by DIR.

CS—Chip select input from the computer. When the host computer wants to initiate either a read or a write cycle, it brings this line high. Read and write cycles are terminated when CS goes low.

DIR—Data direction input from the computer. During a read cycle, this line stays low. During a write cycle, DIR should be driven high.

RDY—Ready output to the computer. Used to indicate to the computer that data is ready during a read cycle or that PLIX has read the data during a write cycle.

Xtal1,Xtal2—Crystal connection. A 3.68-MHz crystal must be connected across these pins. In addition, 15-pF capacitors must be connected from each pin to ground.

N/U—Not used. These pins *must* be connected to Vdd.

## Writing to PLIX

Commands are transmitted to the power line by writing them to PLIX. PLIX controls all timing while sending the message onto the power line, freeing the main processor for other tasks.

Figure 3 details the write cycle timing.

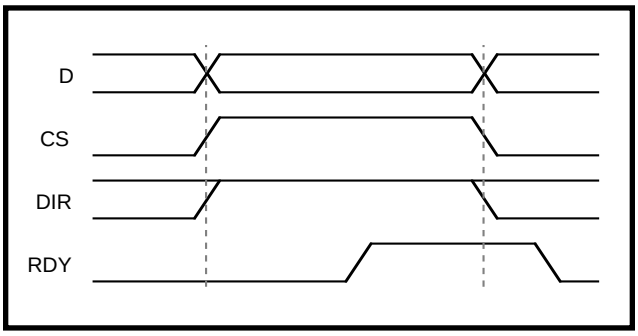



**Figure 3—***PLIX write cycle timing.*

To write a word to PLIX, the main processor first asserts the data (D0–D4) and direction (DIR) lines, then asserts chip select (CS). All lines may optionally be asserted simultaneously. When PLIX has started reading the data, it asserts its ready (RDY) line. When PLIX is finished, it drops RDY to signal the main processor to finish the cycle. A write cycle is concluded when the main processor releases the data, direction, and chip select lines.

Commands are sent to PLIX using three successive writes to the chip, as shown in Figure 4.

| Byte | Function | Range |
|---|---|---|
| 1 | Housecode | 0–15 |
| 2 | Function Code | 0–31 |
| 3 | Repeats | 1–30 |

**Figure 4—***Commands are sent to PLIX using three successive writes to the chip.*

The first word contains the housecode, the second contains the function code, and the third contains a repeat code. All X-10 commands must be repeated twice to ensure the receiving module responds properly. Dim and Bright commands are repeated more than twice to achieve the desired light level. On, Off, All Units Off, and All Lights On commands must be sent to PLIX with a repeat

| Housecode | Decimal | Hexadecimal |
|---|---|---|
| A | 6 | 06 |
| B | 7 | 07 |
| C | 4 | 04 |
| D | 5 | 05 |
| E | 8 | 08 |
| F | 9 | 09 |
| G | 10 | 0A |
| H | 11 | 0B |
| I | 14 | 0E |
| J | 15 | 0F |
| K | 12 | 0C |
| L | 13 | 0D |
| M | 0 | 00 |
| N | 1 | 01 |
| O | 2 | 02 |
| P | 3 | 03 |

| Function | Decimal | Hexadecimal |
|---|---|---|
| 1 | 6 | 06 |
| 2 | 7 | 07 |
| 3 | 4 | 04 |
| 4 | 5 | 05 |
| 5 | 8 | 08 |
| 6 | 9 | 09 |
| 7 | 10 | 0A |
| 8 | 11 | 0B |
| 9 | 14 | 0E |
| 10 | 15 | 0F |
| 11 | 12 | 0C |
| 12 | 13 | 0D |
| 13 | 0 | 00 |
| 14 | 1 | 01 |
| 15 | 2 | 02 |
| 16 | 3 | 03 |
| All Units Off | 16 | 10 |
| All Lights On | 24 | 18 |
| On | 20 | 14 |
| Off | 28 | 1C |
| Dim | 18 | 12 |
| Bright | 26 | 1A |
| All Lights Off * | 22 | 16 |
| Extended Code * | 30 | 1E |
| Hail Request * | 17 | 11 |
| Hail Acknowledge * | 25 | 19 |
| Preset Dim Low * | 21 | 15 |
| Preset Dim High * | 29 | 1D |
| Extended Data * | 19 | 13 |
| Status=On ** | 27 | 1B |
| Status=Off ** | 23 | 17 |
| Status Request ** | 31 | 1F |

* These functions are not currently supported by any X-10 module.
** These functions are presently supported only by the RR501 RF gateway module.

**Figure 5—***Valid X-10 housecodes and function codes.*

code of 2. Dim and Bright commands may be sent with any repeat code from 2 through 30.

When PLIX receives the repeat code, the full command is sent out to the power line. If the main processor initiates another write while PLIX is transmitting, the RDY line will stay low during the first write until the transmission has been completed.

Figure 5 contains all the valid housecodes and function codes that may be sent to PLIX. It is up to the user to ensure the proper codes are being used. PLIX performs no error checking on the commands sent to it.

## Synchronizing the write cycle

The order of the bytes sent to PLIX is very important, so it is equally important that PLIX and the main processor stay in sync. Upon a reset, or at some other interval determined by the programmer, a sync sequence should be performed to coordinate the main processor and PLIX.

A sync sequence consists of sending PLIX three or more zeros, followed by a 31. When PLIX receives the final 31, it expects the next word sent to it to be a housecode.

## Reading from PLIX

PLIX constantly monitors the power line for transmissions and buffers a single received command. The main processor must poll PLIX often enough to ensure no received commands are missed. If there is a potential for a great many consecutive X-10 commands on the power line, PLIX should be polled at least every 300 milliseconds. If there is less X-10 activity taking place, polling may occur less often.

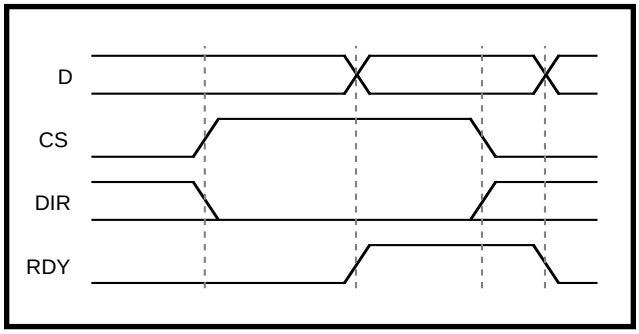



**Figure 6—***PLIX read cycle timing.*

Figure 6 shows the timing for a read cycle.

The main processor starts the read cycle by asserting chip select (CS) while leaving the direction (DIR) line low. When PLIX sees the start of the cycle, it places data on the data (D0–D4) lines and asserts its ready (RDY) line. The main processor then reads the data, and acknowledges by dropping CS. The read cycle is terminated when PLIX removes the data and drops RDY. The main processor should wait until RDY is low before starting a write or another read cycle.

| Byte | Function | Range |
|---|---|---|
| 1 | Housecode | 0–15 |
| 2 | Function Code | 0–31 |

The housecode has a range of 16–31 when a new command has been received. You should subtract 16 from the housecode before decoding it.

**Figure 7—***Commands received from the power line are read by the main processor using a pair of read cycles. Bit 4 of the housecode is set by PLIX to indicate new data. Bit 4 is clear on repeat reads of the same data.*

Two words of data are sent to the main processor by PLIX (see Figure 7). The first word contains the last received housecode and the second word contains the last received function code. There is no way for PLIX to determine how many times a command was transmitted on the power line by other transmitters, so PLIX only reports the last command it heard. As a result, you cannot determine the brightness level of a lamp that has been dimmed or brightened by another transmitter on the same line.

PLIX will repeatedly send the same housecode and function code to the main processor until a new command is received by PLIX from the power line. PLIX signals the main processor to a new command by setting the high bit (D4) of the housecode. After the command has been read once by the main processor, D4 is cleared on any

successive reads. The same command codes shown in Figure 5 also apply to received commands.

## AC Power Fail Detect

In a battery-powered system, the main processor will continue running even if AC power isn't present. The X-10 system requires AC to be present, so the main processor can't send any X-10 commands while AC power is absent. The PLIX ACPFail line indicates the presence or absence of AC power. When the line is high, AC power is present and X-10 comands may be sent. When the line goes low, AC power is absent and no commands will be sent onto the power line. If a write cycle is initiated when AC power isn't present, PLIX won't acknowledge the write (by raising RDY) until after power has been restored.

## PL513/TW523 Connection

The PL513/TW523 uses a standard RJ11-type modular jack to connect to the computer. Figure 8 shows how the connector on the module is numbered. When making the connection to the module, be very careful of modular phone cords that swap conductors end for end. Most modern telephones don't care about the polarity of the connection, so manufacturers of phone cords don't pay any attention when making the cords. If you wire the modular phone connector on the computer end so it matches the wiring of the PL513/TW523, be sure the cable you use passes all signals straight through with no swaps.

One way to check cords that use colored wire internally is to hold both ends side by side with the tabs down so you can see through the plastic connector. If the wire colors go in the same order from left to right, then the cable passes the signals straight through. If the colors of the wires in the connectors go in opposite order, then the cable will swap signal order and it won't work.

If PLIX ever indicates a continuous AC power failure and all connections look correct, double check the modular cable. It is probably swapping the order of the signals.

## Absolute Maximum Ratings

| | |
|---|---|
| Storage temperature | –65°C to +150°C |
| Voltage on any pin with respect to Gnd (except Vdd) | –0.6V to Vdd+0.6V |
| Voltage on Vdd with respect to Gnd | 0 to +9.5 V |
| Total power dissipation | 800 mW |
| Max. current out of Gnd pin | 150 mA |
| Max. current into Vdd pin | 50 mA |
| Max. current into an input pin | ±500 µA |
| Max. output current sinked by any I/O pin | 25 mA |
| Max. output current sourced by any I/O pin | 20 mA |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

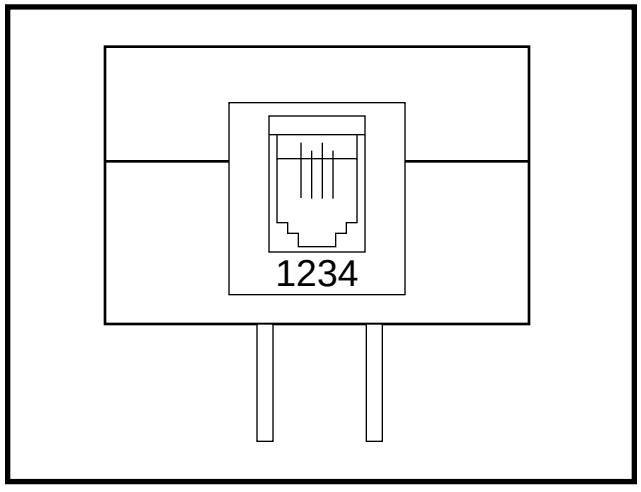



**Figure 8—***PL513/TW523 connector numbering. Pin 1 is the zero crossing output. Pin 2 is ground. Pin 3 is the receiver output on a TW523 or ground on a PL513. Pin 4 is the transmit input.*

## DC Characteristics

Operating temperature 0°C ≤ Ta ≤ +70°C
Operating voltage Vdd = 4.0V to 5.5V

| Characteristic | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| Supply Voltage | 4.0 | | 5.5 | V | |
| Supply Current | | 1.8 | 3.3 | mA | |
| Input Low Voltage | Vss | | 0.2Vdd | V | |
| Input High Voltage | 2.0 | | Vdd | V | |
| Input Leakage Current | –1 | +1 | +1 | µA | |
| Output Low Voltage | | | 0.6 | V | Iol = 9.2 mA, Vdd = 5.5 V |
| | | | 0.6 | V | Iol = 1.6 mA, Vdd = 4.5 V |
| Output High Voltage | Vdd–0.7 | | | V | Ioh = –3.4 mA, Vdd = 5.5 V |
| | Vdd–0.7 | | | V | Ioh = –1.3 mA, Vdd = 4.5 V |

## AC Characteristics

Operating temperature 0°C ≤ Ta ≤ +70°C
Operating voltage Vdd = 4.0V to 5.5V

| Characteristic | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Write Cycle** | | | | | | |
| Data/Direction Setup | Tds | 0 | | | µs | |
| Chip Select to Ready | Trdy | | 11 | 250 | µs | Note 1 |
| Data Hold after Ready | Thold | 0 | | | µs | |
| End of Cycle | Tend | | 8 | 250 | µs | Note 1 |
| **Read Cycle** | | | | | | |
| Data/Direction Setup | Tds | 0 | | | µs | |
| Chip Select to Ready | Trdy | | 12 | 250 | µs | Note 1 |
| Data Hold after Chip Select | Thold | | 7 | 250 | µs | Note 1 |

Note 1: PLIX suspends all bus activity during an X-10 transmission, so a delay of up to 250 µs could occur right after initiating such a transmission.

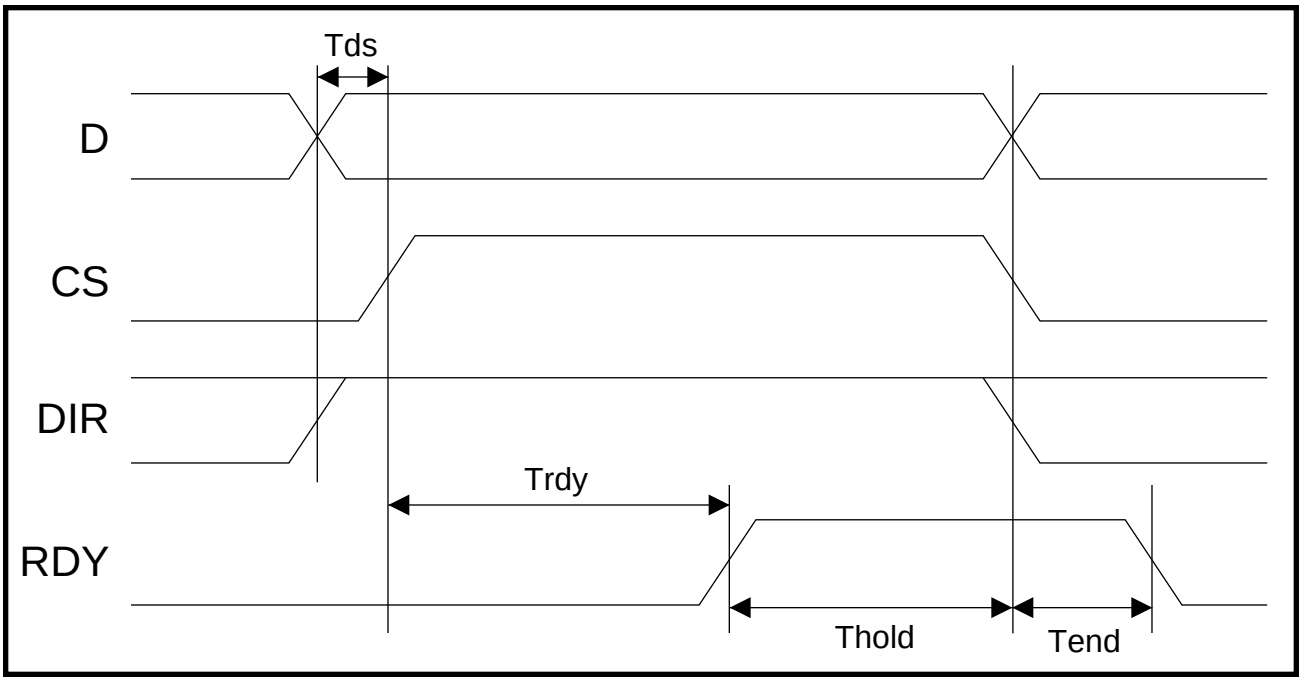



**Figure 9—***Detailed PLIX write cycle timing.*

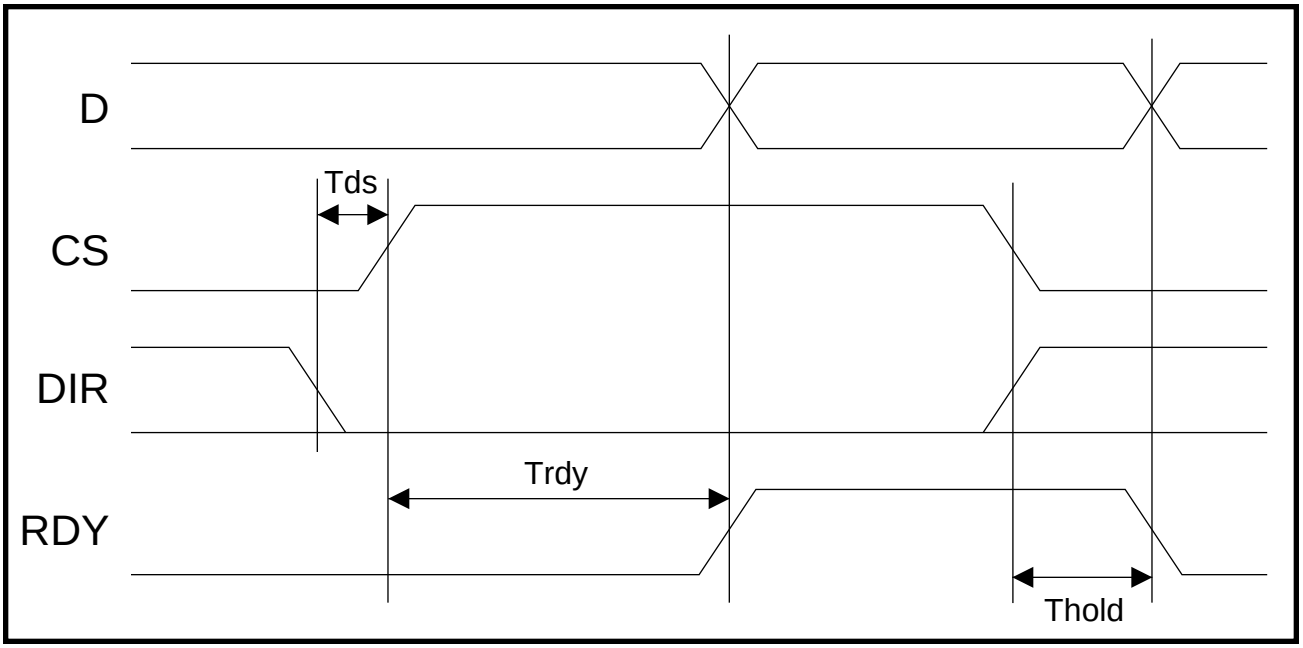
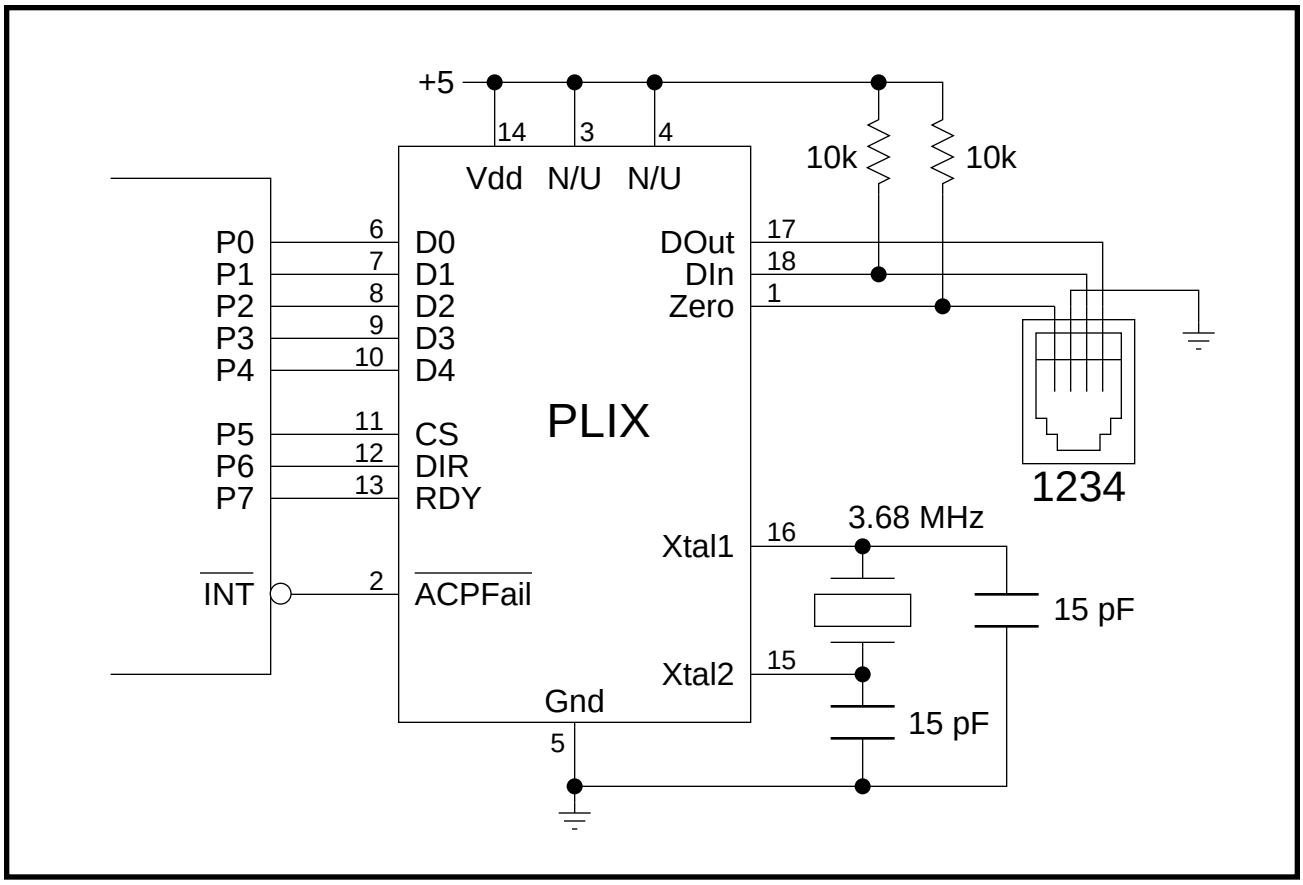



**Figure 10—***Detailed PLIX read cycle timing.*




**Sample Application**

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